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Date: October 21, 2004   By: _Sherry Duncan Bitler_
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of   John Erik LINDHOLM, et al.   Confirmation No.: 7963

Serial No.   10/032,894   Examiner: Thu Thao HAVAN

Filed: 10/26/2001   Art Unit: 2672

FOR: LIGHTING SYSTEM AND METHOD FOR A GRAPHICS PROCESSOR

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Enclosed are the following documents:

[x]   37 C.F.R. § 1.192 Appeal (in triplicate); and
[x]   Return receipt postcard
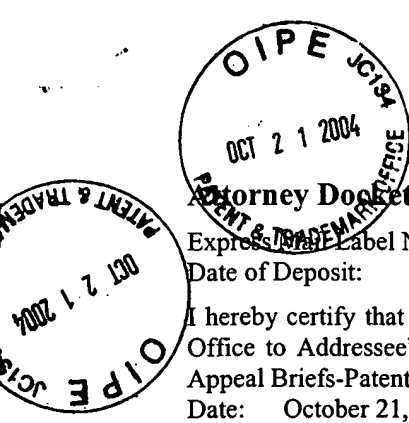
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of John Erik LINDHOLM, et al.   Confirmation No.: 7693

Serial No.   10/032,894   Examiner: Thu Thao HAVAN

Filed: 10/26/2001   Art Unit: 2672

FOR: LIGHTING SYSTEM AND METHOD FOR A GRAPHICS PROCESSOR

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37 C.F.R. § 1.192 APPEAL BRIEF

Sir:

Applicant hereby appeals from the Final Rejection of May 5, 2004 and the Advisory

action of July 12, 2004. The Notice of Appeal was filed on September 7, 2004.

REAL PARTY IN INTEREST

The real party in interest in this appeal is nVIDIA Corporation, as the assignee.

RELATED APPEALS AND INTERFERENCES

There are presently no related appeals or interferences.

STATUS OF CLAIMS

Claims 24-25 and 27-34 are pending. Claims 24, 30, and 34 are independent. The

appendix includes a true copy of all pending claims. No claims have been allowed.

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STATUS OF AMENDMENTS

In the Advisory Action of July 12, 2004, the Examiner indicated that the amendments in the Response filed May 25, 2004 would be entered upon filing this appeal.

SUMMARY OF INVENTION

The technology of the present invention relates to graphics processing and in particular to lighting systems for graphics processing. Although several embodiments of the present invention are disclosed in the lengthy specification, Figure 5 and the supporting text provides a good summary of one of those embodiments. The main text describing Figure 5 is located at page 22 of the specification and portions of that description are reproduced or summarized below. Note that it is not applicants' intention to limit the scope of the invention to what is described in this summary. This material is purely illustrative.

Figure 5, which is reproduced below for convenience, illustrates a lighting system that includes input buffers 400, a memory logic unit (MLU) 500, an arithmetic logic unit (ALU) 504, a register unit 510, an inverse logic unit (ILU) 512, and a conversion module (smearing module) 514. These components and their interconnections are described below.

Referring first to the MLU 500, it has a first input coupled to an output of input buffers 400. As an option, the output of MLU 500 might have a feedback loop 502 coupled to the first input thereof.

As for the ALU 504, it has a first input coupled to an output of MLU 500. In this embodiment, the output of ALU 504 further has a feedback loop 506 connected to the second input thereof. The feedback loop 506 may further have a delay 508 coupled thereto. Coupled to an output of ALU 504 is an input of a register unit 510. It should be noted that the output of register unit 510 is coupled to the first and second inputs of MLU 500.

This embodiment also includes an ILU 512 that includes an input coupled to the output of ALU 504. In an alternate embodiment, ILU 512 might include an input coupled to the output of register unit 510.

Although not always necessary, this embodiment also includes a conversion, or smearing, module 514 coupled between an output of ILU 512 and a second input of MLU 500. In use, the conversion module 514 serves to convert scalar vertex data to vector vertex data. This is accomplished by multiplying the scalar data by a vector so that the vector operators such as the multiplier and/or adder may process it. For example, a scalar A, after conversion, may become a vector (A,A,A,A). In an alternate embodiment, the smearing module 514 might be incorporated into the multiplexers associated with MLU 500, or any other component of the present invention. As an option, a register 516 might be coupled between the output of ILU 512 and an input of the conversion unit 514. Further, such register 516 might be threaded.
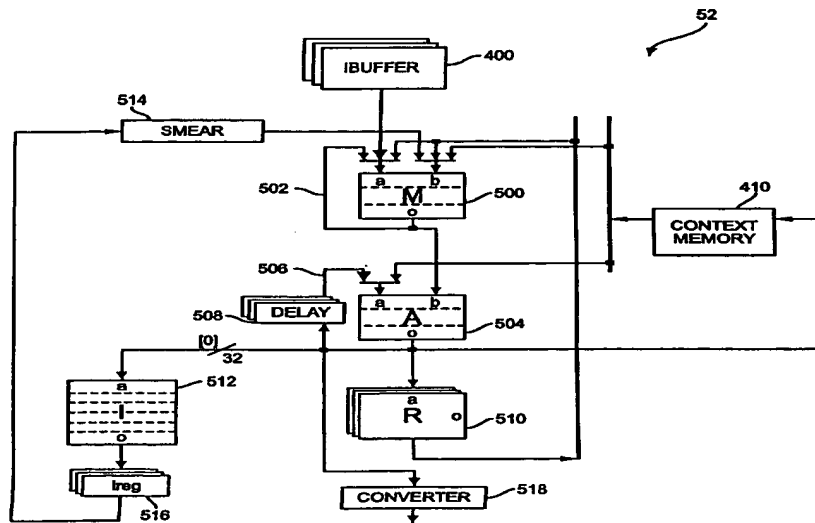

FIG. 5

ISSUES

1) Whether claims 24-25 and 27-34 are anticipated under 35 U.S.C. 102(e) as being unpatentable by Krech (U.S. Patent No. 6,184,902).

GROUPING OF CLAIMS

Claims 24-25 and 27-29 stand or fall together.

Claims 30-34 stand or fall together.

ARGUMENT

Claims 24-25 and 27-29 stand rejected under 35 U.S.C. § 102(e) as being unpatentable by Krech (U.S. Patent No. 6,184,902). This rejection is improper because Krech does not disclose each and every limitation of the claims. For simplicity, independent claim 24 is addressed initially and then independent claims 30 and 34 are addressed jointly.

Independent claim 24

Applicants submit that the 35 U.S.C. § 102 rejection against claim 24 is improper because Krech does not disclose a lighting logic unit that is coupled to a multiplication logic unit via a conversion module adapted for converting scalar vertex data to vector vertex data. Accordingly, the rejection against claim 24 and the corresponding dependent claims should be withdrawn.

Claim 24 is reproduced below for convenience.

24. A lighting system for graphics processing, comprising:

(a)   at least one input buffer adapted for being coupled to a transform system for receiving vertex data therefrom;

(b)   a multiplication logic unit coupled to the at least one input buffer;

(c)   an arithmetic logic unit coupled to the at least one input buffer and the multiplication logic unit;

(d)   a register unit coupled to the arithmetic logic unit; and

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  (e) a lighting logic unit coupled to the arithmetic logic unit, the at least one input buffer, and the multiplication logic unit;

    wherein the lighting logic unit is coupled to the multiplication logic unit via a conversion module adapted for converting scalar vertex data to vector vertex data.

As the claim recites, the lighting logic unit and the multiplication logic unit are coupled by a conversion module that is adapted for converting scalar vertex data to vector vertex data. This limitation was originally part of claim 26, and in the last response, applicants canceled claim 26 and added the subject matter to claim 24.

Krech does not disclose coupling a lighting logic unit and a multiplication logic unit through such a conversion module. In fact, Krech does not even disclose Applicants' claimed conversion module. For example, a simple word search on the Krech patent reveals that it does not once mention any module for converting between scalar vertex data and vector vertex data. Similarly, Krech's figures do not illustrate a conversion module as claimed—much less a lighting logic unit and a multiplication logic unit coupled via a conversion module. Accordingly, Krech cannot be the basis for a proper 35 U.S.C. § 102 rejection of claim 24 or the corresponding dependent claims.

In rejecting claim 24, the advisory action mimics back the language of the claim but never specifically points out the lighting logic unit or the conversion module. Additionally, the advisory action fails to point out the specific connections between the elements of the claim. For example, in rejecting claim 24, the advisory action states:

  Krech discloses lighting logic unit is coupled to the multiplication logic unit via a conversion module adapted for converting scalar vertex data to vector vertex data (fig. 5).

Krech's figure 5 is reproduced below for convenience and is the only material ever cited in the Advisory Action that allegedly shows a lighting logic unit and a multiplication logic unit coupled

via a conversion module. And this material shows no such thing.

Figure 5 identifies over 75 different components. Yet the Advisory Action does not point

to any particular elements that allegedly correspond to the claimed lighting logic unit, the

multiplication logic unit, the conversion module, and the connection between these components.

Instead, the advisory action only points to a multiplier 55. And assuming that the multiplier 55

corresponds to applicants' claimed multiplication logic unit, it can readily be seen from Figure 5

that the multiplier 55 is not connected to a lighting logic unit via a conversion module as

claimed. Accordingly, the rejection against claim 24 cannot properly stand.

FIG. 5
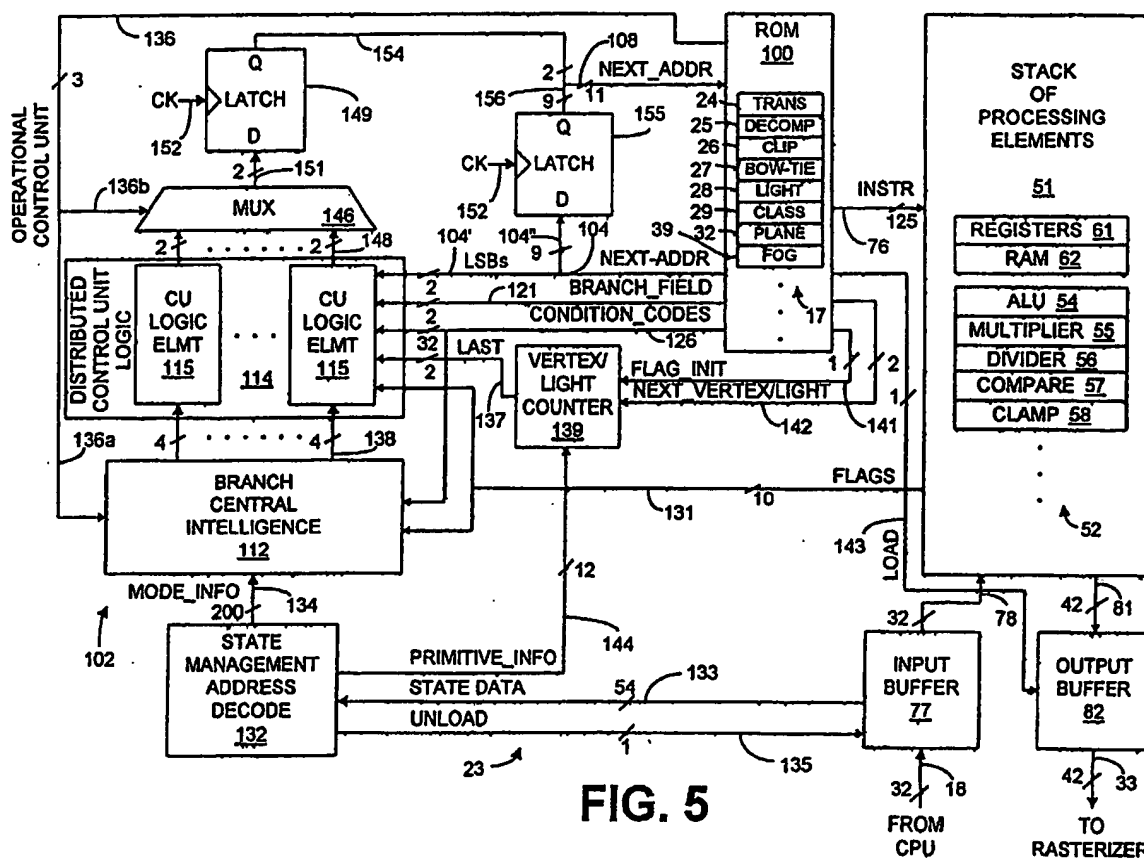
Krech Figure 5

Independent Claims 30 and 34

Applicants submit that the 35 U.S.C. § 102 rejection against claim 30 and 34 is improper because Krech does not disclose a multiplication logic unit that has a feedback loop coupled to an input of the multiplication logic unit. Accordingly, Applicants submit that the rejection against claim 30 and the corresponding dependent claims should be withdrawn. For simplicity, claim 30 is directly addressed, but the same arguments apply to claim 34.

Claim 30 recites a specific architecture for a graphics processing lighting system. That architecture includes several components, including a multiplication logic unit. The claim specifically requires that the multiplication logic unit have a feedback loop coupled to an input of the multiplication logic unit. Claim 30 is reproduced below.

> 30.   A lighting system for graphics processing, comprising:
>
> (a)   at least one input buffer adapted for being coupled to a transform system for receiving vertex data therefrom;
>
> (b)   a multiplication logic unit coupled to the at least one input buffer;
>
> (c)   an arithmetic logic unit coupled to the at least one input buffer and the multiplication logic unit;
>
> (d)   a lighting logic unit coupled to the arithmetic logic unit, the at least one input buffer, and the multiplication logic unit; and
>
> (e)   memory coupled to the multiplication logic unit and the arithmetic logic unit;
>
> wherein the multiplication logic unit has a feedback loop coupled to an input of the multiplication logic unit.

Krech does not teach or disclose a multiplication logic unit with a feedback loop as claimed. As previously discussed, Krech discloses a multiplier 55 that is shown in Figure 5. Figure 5 does not illustrate any type of feedback loop coupled to an input of the multiplier 55.

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Thus, Figure 5 cannot support the rejection.

In rejecting claims 30 and 34, the advisory action points to column 11, line 45 through column 13, line 15 and Figure 7. Additionally, the advisory action states:

> Krech teaches a vertex looping routing is commenced, which processes data associated with a vertex of the primitive during each loop operation. The appropriate control unit logic element determines via the last vertex bit whether the vertex that was recently operated on in the past by the stack is the last vertex of the primitive that is currently at issue.

There is no mention in the rejection of a multiplication logic unit or a feedback loop coupled to the input of the multiplication logic unit. The advisory action does not even address any architectural features of the graphics processing system. Instead, the advisory action points to a software routine. For example, Krech Figures 7a and 7b are flowcharts of software methods.
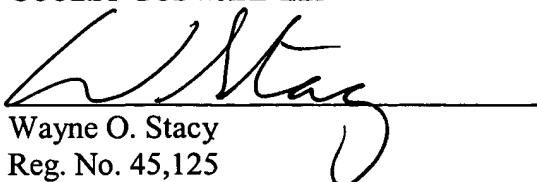
The material cited in the advisory action does not anticipate the architectural limitations set forth in claims 30 and 34. Accordingly, applicants submit that the 102 rejection against claim 30 and 34 is improper because Krech, at the very least, does not disclose a multiplication logic unit that has a feedback loop coupled to an input of the multiplication logic unit.

SUMMARY

All of the pending claims are patentable for the reasons set forth herein, and Appellant respectfully requests such finding.

Three copies of this Appeal Brief are provided along with payment of the required fee.

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APPENDIX

CLAIMS ON APPEAL

24.   A lighting system for graphics processing, comprising:

(a)   at least one input buffer adapted for being coupled to a transform system for receiving vertex data therefrom;

(b)   a multiplication logic unit coupled to the at least one input buffer;

(c)   an arithmetic logic unit coupled to the at least one input buffer and the multiplication logic unit;

(d)   a register unit coupled to the arithmetic logic unit; and

(e)   a lighting logic unit coupled to the arithmetic logic unit, the at least one input buffer, and the multiplication logic unit;

wherein the lighting logic unit is coupled to the multiplication logic unit via a conversion module adapted for converting scalar vertex data to vector vertex data.

25. The system as recited in claim 24, wherein the multiplication logic unit has a feedback loop coupled to an input thereof.

27. The system as recited in claim 24, wherein the arithmetic logic unit and the multiplication logic unit include multiplexers.

28. The system as recited in claim 24, wherein the multiplication logic unit includes three multipliers coupled in parallel.

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29. The system as recited in claim 24, wherein the arithmetic logic unit includes three adders coupled in series and parallel.

30. A lighting system for graphics processing, comprising:

(a)   at least one input buffer adapted for being coupled to a transform system for receiving vertex data therefrom;

(b)   a multiplication logic unit coupled to the at least one input buffer;

(c)   an arithmetic logic unit coupled to the at least one input buffer and the multiplication logic unit;

(d)   a lighting logic unit coupled to the arithmetic logic unit, the at least one input buffer, and the multiplication logic unit; and

(e)   memory coupled to the multiplication logic unit and the arithmetic logic unit;

wherein the multiplication logic unit has a feedback loop coupled to an input of the multiplication logic unit.

31. The system as recited in claim 30, wherein the memory includes a plurality of constants for processing the vertex data.

32. The system as recited in claim 30, wherein the memory has a read terminal coupled to the multiplication logic unit.

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33. The system as recited in claim 30, wherein the memory has a write terminal coupled to the arithmetic logic unit.

34. A lighting system for graphics processing, comprising:

    (a)   a multiplication logic unit;

    (b)   an arithmetic logic unit coupled to the multiplication logic unit;

    (c)   a register unit coupled to the arithmetic logic unit;

    (d)   a lighting logic unit coupled to the arithmetic logic unit and the multiplication logic unit; and

    (e)   memory coupled to the multiplication logic unit and the arithmetic logic unit;

wherein the multiplication logic unit has a feedback loop coupled to an input of the multiplication logic unit.